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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,902	08/11/2000	Kozo Harada	50090-234	8376

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EXAMINER
CHU, CHRIS C

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/635,902	HARADA ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3, 4, 6, 8, 9 and 12 - 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3, 4, 6, 8, 9 and 12 - 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *21 November 2001* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment filed on November 21, 2001 has been received and entered in this office action.

Cancel claims: 1, 2, 5, 7, 10 and 11.

Amend claims: 3, 4, 6, 8, 9, 12, 13, and 15.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 3, 8 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakamoto et al.

Note Fig. 5 of Sakamoto et al., where he/she shows a semiconductor device comprising: a semiconductor chip (300); at least a first electrode (310) formed on the first major surface of said semiconductor chip, at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface (see Fig. 5); and at least a conductive member (306) for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip (see Fig. 5), wherein each of said conductive members (306) is comprised of a conductive clip holding said first electrode together with said second electrode or said insulation layer (see Fig. 5), said conductive clip having elasticity for clamping objects.

Regarding claim 8, note Fig. 5 of Sakamoto et al., where he/she shows a semiconductor device comprising: a plurality of semiconductor device units (see Fig. 5), each of said semiconductor device units including: a semiconductor chip (300); at least a first electrode (310) formed on the first major surface of said semiconductor chip (see Fig. 5), at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface (see Fig. 5); and at least a conductive member (306) for connecting said first electrode with said second electrode or said insulation layer (see Fig. 5), said conductive member (306) being formed along the outer circumference of at least a side of said semiconductor chip (see Fig. 5); wherein said semiconductor device units are stacked each other, and said conductive members are connected to each other (see Fig. 5), wherein each of said conductive members

(306) is comprised of a conductive clip holding said first electrode together with said second electrode or said insulation layer, said conductive clip having elasticity for clamping objects.

Regarding claim 12, note Fig. 5 of Sakamoto et al., where he/she shows a semiconductor device comprising: a plurality of semiconductor device units (see Fig. 5), each of said semiconductor device units including: a semiconductor chip (300); at least a first electrode (310) formed on the first major surface of said semiconductor chip (see Fig. 5), at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface (see fig. 5); and at least a conductive member (306) for connecting said first electrode with said second electrode or said insulation layer (see Fig. 5), said conductive member (306) being formed along the outer circumference of at least a side of said semiconductor chip (see Fig. 5); a packaging board (320) for mounting said plurality of semiconductor device units (see Fig. 5); wherein said semiconductor device units are placed on said packing board so as to have a predetermined angle to said packaging board (see Fig. 5), and said conductive members (306) of said semiconductor device units are connected to said packaging board (see Fig. 5), wherein each of said conductive members (306) is comprised of a conductive clip holding said first electrode together with said second electrode or said insulation layer (see Fig. 5), said conductive clip having elasticity for clamping objects.

4. Claim 6 is rejected under 35 U.S.C. 102(e) as being anticipated by Gaynes et al.

Note Figs. 8A and 8B of Gaynes et al., where he/she shows a semiconductor device comprising: a plurality of semiconductor device units (see Figs. 8A and 8B), each of said semiconductor device units including: a semiconductor chip (85); at least a first electrode (read

column 10, lines 55 ~ 67) formed on the first major surface of said semiconductor chip (see Figs. 8A and 8B), at least a second electrode or an insulation layer (read column 10, lines 55 ~ 67; column 11, lines 1 ~ 6 and see Fig. 17) formed on the second major surface opposite to said first major surface (see Figs. 8A, 8B and 17); and at least a conductive member (84 and read column 10, lines 60 and 61) for connecting said first electrode with said second electrode or said insulation layer (see Figs. 8A and 8B), said conductive member (84) being formed along the outer circumference of at least a side of said semiconductor chip (see Figs. 8A and 8B); wherein said semiconductor device units are stacked on each other (see Figs. 8A and 8B), wherein a first chip has a first conducting pattern extended from said first electrode (see Figs. 8A and 8B), a second chip has a second conducting pattern extended from said second electrodes (see Figs. 8A and 8B), and a bump (81) is provided between said first conducting pattern and said second conducting pattern (see Figs. 8A and 8B), which face to each other, for electrically connecting said two conducting patterns (read column 11, lines 6 ~ 10).

5. Claims 14 ~ 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Akram et al.

Note Fig. 4 of Akram et al., where he/she shows a semiconductor device comprising: a plurality of semiconductor chips (14) each having electrodes formed on the major surface thereof (see Fig. 4), and a plurality of spacer members (10A, 10B, and 10C) each having conductive pattern on the surface thereof (see Fig. 4); wherein said semiconductor chips (14) and said spacer members (10A ~ 10C) are stacked (see Fig. 4) alternately such that said electrodes of said semiconductor chips are electrically connected to said conductive patterns of said spacer

members, and said conductive patterns of said spacer members are electrically connected to each other (see Fig. 4).

Regarding claim 15, note Fig. 4 of Akram et al., where he/she shows each of said spacer members has a cavity for accommodating the end portion of said semiconductor chip, said end portion is located at least partially within the cavity (see Fig. 4).

Regarding claim 16, note Fig. 4 of Akram et al., where he/she shows further comprising supporting members having conductive pattern thereon, wherein said supporting members are placed so as to make said conductive patterns thereof contact with said conductive patterns of said plurality of spacer members (see Fig. 4).

6. Claims 14 ~ 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Sugano et al.

Note Fig. 46 of Sugano et al., where the reference shows a semiconductor device comprising: a plurality of semiconductor chips (302 in Fig. 47) each having electrodes (304 in Fig. 47) formed on the major surface thereof (see Fig. 46), and a plurality of spacer members (310 and 314 in Fig. 47) each having conductive pattern on the surface thereof (see Fig. 46); wherein said semiconductor chips (302 in Fig. 47) and said spacer members (310 and 314 in Fig. 47) are stacked (see Fig. 46) alternately such that said electrodes (304 in Fig. 47) of said semiconductor chips (302 in Fig. 47) are electrically connected (304 in Fig. 47) to said conductive patterns of said spacer members, and said conductive patterns of said spacer members are electrically connected to each other (see Fig. 46).

Regarding claim 15, note Fig. 46 of Sugano et al., where the reference shows each of said spacer members (310 and 314 in Fig. 47) has a cavity for accommodating the end portion of said semiconductor chip, said end portion is located at least partially within the cavity (see Fig. 46).

Regarding claim 16, note Fig. 46 of Sugano et al., where the reference shows further comprising supporting members having conductive pattern thereon (see Fig. 47), wherein said supporting members are placed so as to make said conductive patterns thereof contact with said conductive patterns of said plurality of spacer members (see Fig. 46).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4, 9, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al. in view of Whitney et al.

Sakamoto et al. discloses the claimed invention except each of said conductive members is comprised of a conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer. However, Whitney et al. shows that a conductive layer (70 and 80 in Fig. 1) to bond the first electrode and second electrode. Thus, it would have been obvious to one of ordinary skill in the art at the time when

the invention was made to modify Sakamoto et al. by using a conductive layer as taught by Whitney et al. The ordinary artisan would have been motivated to modify Sakamoto et al. in the manner described above for at least the purpose of increasing reliability and operation of the package (column 1, lines 26 ~ 31).

Response to Arguments

9. Applicant's arguments with respect to claim 6 have been considered but are moot in view of the new ground(s) of rejection.

10. Applicant's arguments with respect to claims 3, 4, 8, 9 and 12 ~ 16, which are filed on November 21, 2001 have been fully considered but they are not persuasive.

Applicant's arguments against Sakamoto et al. have been fully considered but they are not deemed to be persuasive since the claimed limitation "the clip having elasticity for clamping objects" is readable on the structure of Sakamoto et al. In Fig. 5 of Sakamoto et al., note that solder ball (308) takes the form of leads (306). That is note the depression formed in the solder ball by lead (306). This clearly suggests that the lead (306) have elasticity for clamping object (300).

On page 12, paragraph 2, applicant states "the alleged conductive layer 70/80 does not connect electrodes on opposing sides of a substrate ..., rendering the alleged conductive layer 70/80 immaterial to the claimed "conductive layer" both structurally and functionally (as well as non-analogous to the lead 306 of Sakamoto et al.)"

a. In response to applicant's argument that Whitney et al. is non-analogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Whitney et al. and Sakamoto et al. are analogous art because they are from the same field of endeavor, that is the semiconductor device.

b. In response to applicant's argument that "the alleged conductive layer 70/80 [is] immaterial to the claimed 'conductive layer' both structurally and functionally." This is not persuasive because the material of the conductive layer 70/80 is an electrically conductive material. See Whitney et al. column 4, lines 51 ~ 59 where he/she discloses silver, nickel, and lead/tin. Therefore, the combination of Sakamoto et al. in view of Whitney et al. does not change the principle of operation of the Sakamoto et al., and is in fact operable for its intended purpose.

c. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971) references are evaluated by what

they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA 1969).

d. In response to applicant's argument on page 14, paragraph 2 that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this case, Whitney et al. clearly discloses or teaches the desirability of modifying Sakamoto et al. as set forth in the 103 rejections. For instance, see column 1, lines 26 ~ 31.

On page 16, paragraph 2, applicant states "it appears that the device of Akram et al. does not have electrically connecting electrodes to conductive patterns, whereby the conductive patterns are electrically connected to each other as recited in claim 14." Examiner dose not concur. Because Akram et al. clearly discloses that the electrodes (24 in Fig. 1) which is electrically connected to the conductive patterns (26 in Fig. 1 and see Fig. 4). Furthermore, the applicant's argument against "supporting members" has been fully considered but they are not persuasive. Since "supporting members" is not clearly defined in the claim, any structure that is supporting the semiconductor device is read as the "supporting members." In Fig. 4 of Akram et al., where he/she shows the spacer members (10A, 10B, and 10C), which has a protrusion part,

and the protrusion part of the spacer members is supporting the semiconductor device. Therefore, Akram et al. discloses the "supporting members" as recited in claim 16.

On page 17, paragraph 2, applicant states "it appears that the device of Sugano et al. does not have electrically connecting electrodes to conductive patterns, whereby the conductive patterns are electrically connected to each other as recited in claim 14." Examiner dose not concur. Because Sugano et al. clearly discloses that the electrodes (304 in Fig. 47) which is electrically connected to the conductive patterns (see Figs. 46 and 47). Furthermore, the applicant's argument against "supporting members" has been fully considered but they are not persuasive. Since "supporting members" is not clearly defined in the claim, any structure that is supporting the semiconductor device(s) is read as the "supporting members." In Figs. 46 and 47 of Sugano et al., where he/she shows a substrate (336), which is supporting the semiconductor device(s). Therefore, Sugano et al. discloses the "supporting members" as recited in claim 16.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
February 25, 2002

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